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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,961	02/11/2004	Ho-Young Lee	SAM-0521	3562

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/776,961	LEE, HO-YOUNG	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,14-18 and 27* is/are rejected.

7)☒ Claim(s) *6-13 and 19-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 10, 21 and 23 are objected to because of the following informalities:

Claims 10 and 23, line 2, "with third transistors" should be changed to --with the third transistor--.

Claim 21, line 2, "parallel the" should be changed to --parallel with the--.

Appropriate correction to the above informalities is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu (USP 6,043,699).

With respect to claims 1-5, Figure 7 of the Shimizu reference discloses a level shifting device, which includes: a first transistor (NMOS NT1), an input signal (Tin), a voltage node at a lower voltage value (ground), an output signal (Tout); a second transistor (NMOS NT2), an inverted version of the input signal (output of inverter I1), an inverted version of the output signal (at the junction connection of PT2 and NT2); a third transistor (PMOS PT1); a fourth transistor (PMOS PT2), a voltage supply at a first upper voltage value (power supply having 6V); and a fifth transistor (PMOS PT3); wherein the input signal (Tin) swings between a second upper voltage value (3V) and the lower voltage value (ground), and the output signal (Tout) swings between the first upper voltage value (6V) and the lower voltage value (ground). Also, Figure 7 shows the level shifter device including a sixth transistor (PMOS PT4)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 14-18 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (USP 6,043,699) in view of Hayashi et al. (US 2002/0050849 A1).

With respect to claims 14-18, Figure 7 of the Shimizu reference discloses a level shifting device which includes all of the limitations of these claims, as discussed in the 102 rejections of claim 1-5 above, except for a latch circuit receiving the output signal and the inverted version of

the output signal. However, Figure 1 of the Hayashi et al. reference discloses a level shifting device that includes a latch circuit (13, 14, 15) receiving the output signal (n1) and the inverted version (n2) of the output signal of the level shifter unit (11-12) for the purpose of improving the speed and the performance of circuitry (see page 7, paragraphs [0073]-[0077]). Therefore, it would have been obvious to one having skills in the art at the time the invention was made to modify the level shifter in Figure 7 of the Shimizu reference by providing the level shifter in Figure 7 of the Shimizu reference with the latch circuit receiving the output signal and the inverted version of the output signal of the level shifter unit as taught in Figure 1 of the Hayashi et al. reference for the purpose of improving the speed and the performance of the circuitry. Thus, this combination/modification meets all the limitations of claims 14-18.

With respect to claim 27, the latch circuit (13-15, Figure 1 of Hayashi et al.) in the above combination/modification comprises a CMOS transistor configuration (because the latch circuit in Figure 1 of the Hayashi et al. is formed by using PMOS and NMOS transistors).

Allowable Subject Matter

7. Claims 6-13 and 19-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 7, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816